Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 43, No. 2(2013), 124 – 130

Simulation of semiconductor bulk trap influence on the electrical characteristics of the n-channel power VDMOS transistor

Sanja Aleksić, Biljana Pešić and Dragan Pantić

Department of Microelectronics, Faculty of Electronic Engineering, University of Niš, Niš, Serbia,

Abstract: In this paper the impact of traps generated in semiconductor bulk due to High Electric Field Stress (HEFS) or irradiation of n-channel power VDMOSFET are presented. The influence of semiconductor bulk traps is expected, due to the fact that the current mainly flows vertically through the n-epitaxial layer and n+ substrate to drain contact. For the reverse engineering of the process flow and the simulation of electrical characteristics of power VDMOS transistor, Technology Computer-Aided Design (TCAD) software package tools from Silvaco are used. Taking the advantage of simulation, the influences of donor (DT) and acceptor (AT) traps generated in the semiconductor bulk on the electrical characteristics are separately analysed and discussed.

Key words: TCAD, power VDMOSFET, donor and acceptor bulk traps

Simulacija vpliva pasti v substratu n kanalnega močnostnega VDMOS tranzistorja na njegove električne lastnosti

Povzetek: V članku so predstavljeni vplivi pasti v substratu n kanalnega močnostnega VDMOS tranzistorja zaradi sevanja ali vpliva visokega električnega polja (HEFS). Vpliv pasti se pričakuje zaradi vertikalnega toka preko epitaksijske plasti n in n+ substrata v kontakt. Za analizo električnih lastnosti tranzistorja je bila uporabljena TCAD programska oprema proizvajalca Silvaco. Simulacije omogočajo, da je vpliv akceptorskih in donorskih plasti obravnavan ločeno.

Ključne besede: TCAD, močnostni VDMOSFET, donorske in akceptorske pasti v substratu

** Corresponding Author's e-mail: sanja.aleksic@elfak.ni.ac.rs*

1 Introduction

The advanced generation of power VDMOS transistors are designed for a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired. These components are widely used in various applications. Considering the facts that the design of highly reliable, high-speed and low power integrated circuits (IC) is the critical task in this procedure, it is very important to know how the power VDMOS transistor acts when it is exposed to various stresses, such as high electrical field stress or irradiation. In this cases the defects in the form of traps (which can be neutral or charged), are generated in oxide and semiconductor bulk, as well as at the Si/SiO_2 interface. They significantly influence on the electrical characteristics of semiconductor devices. The traps, generated at the Si/SiO_2 interface and in the gate oxide, have the dominant influence on the electrical characteristics of MOS transistors [1-7], while in the power VDMOS transistor the influence of generated traps in semiconductor bulk must be taken into account due to the fact that the current mainly flows vertically through the n-epitaxial layer and n^+-substrate to drain contact. Further reducing in VDMOS transistor size continually complicates the device physics and makes device modeling more sophisticated [8-10]. Because of that, complete fabrication process flow and device electrical characteristics simulation programs, as well as the

electronic circuit simulators, are the essential tools in the procedure of ICs design.

Over the last thirty years a number of papers and reports dealing with the degradation of the electrical characteristics of semiconductor devices due to different stress conditions have been published, where the physical models for the instability explanations has proposed [11-15]. In the most of these models, the presence of defects in semiconductor substrates was neglected, because in standard MOS structures the defects generated in the gate oxide and the Si/SiO_2 interface have the dominant influence on the electrical characteristics. In VDMOS structures their influence could not be ignored, because of vertical current flow. Using the possibilities provided by TCAD simulation tools for separation of different parameters influence, models and mechanisms on the device electrical characteristics, in this paper only the effects of semiconductor bulk traps on the electrical characteristics of n-channel power VDMOS transistor are investigated. The basic data necessary for the power VDMOSFET electrical characteristics simulation is the net doping profile distribution in its two-dimensional (2D) simulation domain. It is determine by the procedure of reverse engineering within the values of basic process parameters are determined on the basis of available information obtained from literature, data sheets and measurements, and the simulation of the complete power VDMOSFET production process flow by using ATHENA process simulator [16]. Afterwards, the electrical characteristics of VDMOS transistors and the influence of bulk trap generation mechanisms on them are simulated by using the device simulator ATLAS [17]. The semiconductor bulk trap mathematical model incorporated in the device simulator ATLAS is given in the second part of this paper. Finally, the obtained simulation results are analyzed, where the impacts of donor-like and acceptor-like semiconductor bulk traps are considered separately.

2 Semiconductor bulk trap mathematical models

The presence of defects in semiconductors (impurities, vacancies, dangling bonds, etc.) has a significant impact on the device electrical characteristics, especially when these defects are charged. These traps are changing the density of space charge and the potential distribution in the device structure and also have the influence on the recombination statistics and carriers mobility. The fact is that the amount of bulk and interface charged traps increases significantly when the devices are exposed to high electric field or radiation [3, 8], and in these cases, accurate simulation of the electrical characteristics of semiconductor devices requires to take into consideration the influence of space charge that comes from stress induced charge traps.

In solid-state physics there are three different mechanisms which add space charge directly into the right hand side of Poisson's equation in addition to the ionized donor and acceptor impurities, and these are interface fixed charge, interface trap and bulk trap states. Interface fixed charge Q_f is modeled as a sheet charge at the Si/SiO_2 interface and therefore is controlled by the interface boundary condition, while interface traps Q_{IT} and semiconductor bulk traps Q_{BT} add space charge directly into the Poisson's equation:

$$div(\varepsilon\nabla\varphi) = q(n - p - N_D^+ + N_A^-) - (Q_{IT} + Q_{BT}) \quad (1)$$

This section describes the definition of bulk trap states mathematical models that are implemented in program ATLAS that provides general capabilities for physically-based 2D and 3D simulation of semiconductor devices [17].

2.1 Bulk trap implementation into Poisson equation

Associated energy of bulk traps lies in the forbidden gap and exchange charge with the conduction and valence band through the emission and capture of electrons and holes, as it is shown in Fig. 1. They can be donor-like trap (DT) or acceptor-like trap (AT). DT filled with electron is neutral and with the release of an electron becomes positive charged (ionized). Unlike donors, the energy level for DT lies in energy gap near the top of valence band. Contrary, empty AT is neutral and becomes negatively charged (ionized) when filled with an electron. His energy level lies near the bottom of conduction band [17].

The net charge due to the presence of traps in semiconductor bulk is added on the right hand side of Poisson's equation. The total space charge is defined as:

$$Q_{BT} = q(N_{DT}^+ - N_{AT}^-) = Q_{DT}^+ - Q_{AT}^- \quad (2)$$

N^+_{DT} and N^-_{AT} are the densities of ionized DT and AT, respectively, and their densities are equal to the product of the donor-like trap densities N_{DT} and acceptor-like trap densities N_{AT} in the semiconductor bulk and its probability of ionization F_{DT} and F_{AT}.

$$N_{DT}^+ = N_{DT} \cdot F_{DT} \quad (3)$$

$$N_{AT}^{-} = N_{AT} \cdot F_{AT} \quad (4)$$

The probability of ionization assumes that the capture cross sections are the constant for all trap energy levels in the forbidden band, and follows the analysis developed by Simmons and Taylor [18]:

$$F_{DT} = \frac{v_p \sigma_p p + e_{nD}}{v_n \sigma_n n + v_p \sigma_p p + e_{nD} + e_{pD}} \quad (5)$$

$$F_{AT} = \frac{v_n \sigma_n n + e_{pA}}{v_n \sigma_n n + v_p \sigma_p p + e_{nA} + e_{pA}} \quad (6)$$

σ_n and σ_p are electron and hole capture cross sections, respectively, ν_n and ν_p are the thermal velocities for electron and hole, while the electron and hole emission rates for DT, e_{nD} and are e_{pD} defined by:

$$e_{nD} = \frac{1}{D.FAC} \cdot v_n \cdot \sigma_n \cdot n_i \cdot \exp\left(\frac{E_T - E_i}{kT_L}\right) \quad (7)$$

$$e_{pD} = D.FAC \cdot v_p \cdot \sigma_p \cdot n_i \cdot \exp\left(\frac{E_i - E_T}{kT_L}\right) \quad (8)$$

E_i is the intrinsic Fermi level position, E_T is the energy of the discrete trap level, and T_L is the lattice temperature. Parameter D.FAC takes into account the fact that defects in "empty" or "filled" conditions have different spin and degeneracy.

The emission rates for AT, e_{nA} and e_{pA} are defined by:

$$e_{nA} = D.FAC \cdot v_n \cdot \sigma_n \cdot n_i \cdot \exp\left(\frac{E_T - E_i}{kT_L}\right) \quad (9)$$

$$e_{pA} = \frac{1}{D.FAC} \cdot v_p \cdot \sigma_p \cdot n_i \cdot \exp\left(\frac{E_i - E_T}{kT_L}\right) \quad (10)$$

In the case when several different donor and/or acceptor trap energy levels are defined, the net space charge is the sum of charges originated from all defined traps.

In order to activate semiconductor bulk trap model in ATLAS device simulation tool and to analyze DT and AT impact on electrical characteristics of semiconductor device TRAP statements is used. The accurate simulation of device physics requires the use of transient trap simulation model, since DT and AT do not reach the equilibrium distribution instantly, but require time for electrons to be emitted or captured. However, this simulation is time consuming and therefore the static model is often used.

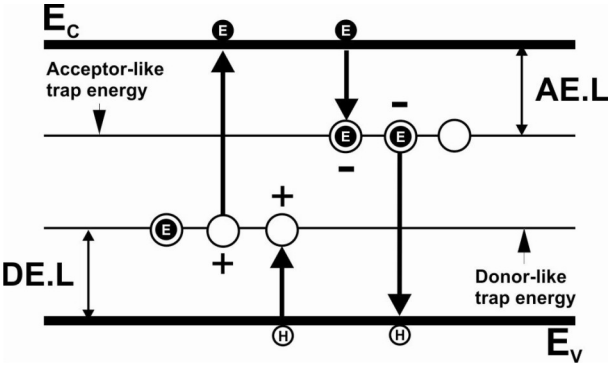

Figure 1: Donor and acceptor trap energy levels and charge states in Si forbidden gap.

2.2 Bulk trap implementation into recombination model

The presence of defects in the semiconductor bulk can significantly affects on the concentration of carriers because that electrons are being emitted or captured by DT and AT. This is accounted in the carrier continuity equations by modifying the standard Shockley-Read-Hall recombination term as follows [19]:

$$R_{SRH} = \sum_{i=1}^{A} R_{Di} + \sum_{i=1}^{B} R_{Aj} \quad (11)$$

where A is the number of DT energy levels in the forbidden gap, B is the number of AT energy levels in the forbidden gap, while their recombination terms R_D and R_A are:

$$R_D = \frac{pn - n_i^2}{\tau_p\left[n + \frac{1}{D.FAC} \cdot n_i \cdot \exp\left(\frac{E_{TD} - E_i}{kT_L}\right)\right] + \tau_n\left[p + D.FAC \cdot n_i \cdot \exp\left(\frac{E_i - E_{TD}}{kT_L}\right)\right]} \quad (12)$$

$$R_A = \frac{pn - n_i^2}{\tau_p\left[n + D.FAC \cdot n_i \cdot \exp\left(\frac{E_{TA} - E_i}{kT_L}\right)\right] + \tau_n\left[p + \frac{1}{D.FAC} \cdot n_i \cdot \exp\left(\frac{E_i - E_{TA}}{kT_L}\right)\right]} \quad (13)$$

E_{TD} and E_{TA} are the donor and acceptor trap energies, E_i is the intrinsic Fermi level and T_L is the lattice temperature. The electron and hole lifetimes τ_n and τ_p are related to the carriežr cross sections σ_n and σ_p through equations:

$$\tau_n = \frac{1}{\sigma_n \cdot v_n \cdot N_{DT}} \quad (14)$$

$$\tau_p = \frac{1}{\sigma_p \cdot v_p \cdot N_{AT}} \quad (15)$$

ν_n and ν_p are the thermal velocities for electron and holes, respectively.

3 Simulation results

In this section the impacts of DT and AT traps in semiconductor bulk on the electrical characteristics of power n-channel VDMOS transistor from IRF510 serial are presented. This device is intentionally used, since its drain current after the channel, flows vertically through the n-epitaxial layer and substrate (Fig. 2.), and therefore the impact of the semiconductor bulk traps on the device electrical characteristics is more pronounced. The simulations have been carried out by using the process simulator ATHENA [16] and the device simulator ATLAS [17], which are the integral part of Silvaco TCAD software package. The reverse engineering of the complete production process flow of the power VDMOS transistor is made by the using of the available technical documentation and its measured electrical characteristics.

3.1 Reverse engineering of power VDMOSFET's process flow

TCAD study of semiconductor bulk traps influence on the electrical characteristics is done on the n-channel power VDMOS transistor IRF510. This transistor is the third advanced generation HEXFETs from International Rectifier, designed for a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired. For the simulation of its electrical characteristics the doping profile distribution in the 2D simulation domain is required. Determination of the doping profile is a serious problem due to the complex structure of the device (Fig. 2) and the fact that the complete technology production flow of power VDMOS transistor has more than hundred process steps, where each process has several parameters that are unknown.

At the beginning of the process simulation the initial data that we know are: the basic information about used technology (substrate concentration epitaxial layer concentration and thickness, source/drain and well regions junction depths and sheet resistances, and the order of process steps in the production flow), design rules for the given technology, information from IRF510 data sheet [20] (threshold voltage V_{TH}, gate oxide thickness channel length, drain to source on-resistance transfer and output electrical characteristics) and measured electrical characteristics of power VDMOS transistor (V_{TH} = 2.7 V, $I_D = f(V_{GS})$, $I_D = F(V_{DS})$).

The production process flow is reconstructed by using all this data and information about device geometry, and the values of process parameters such as: implantation doses and energies, time and temperature of diffusion and oxidation processes, etc., are determined.

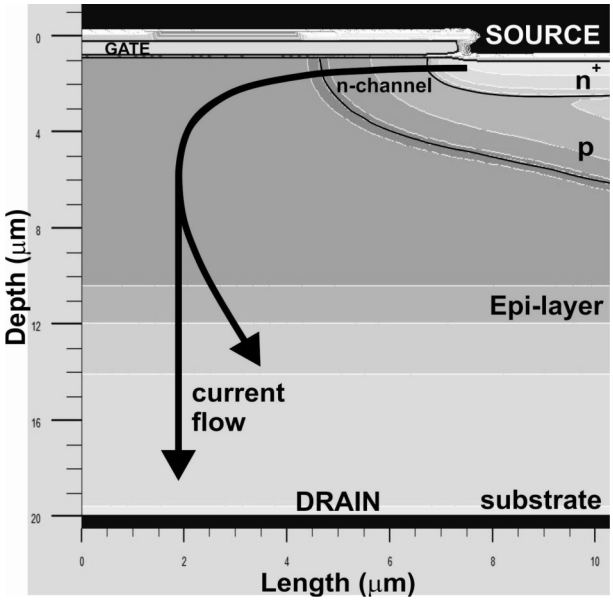

Figure 2: The cross-section and 2D simulation domain of the power VDMOS transistor.

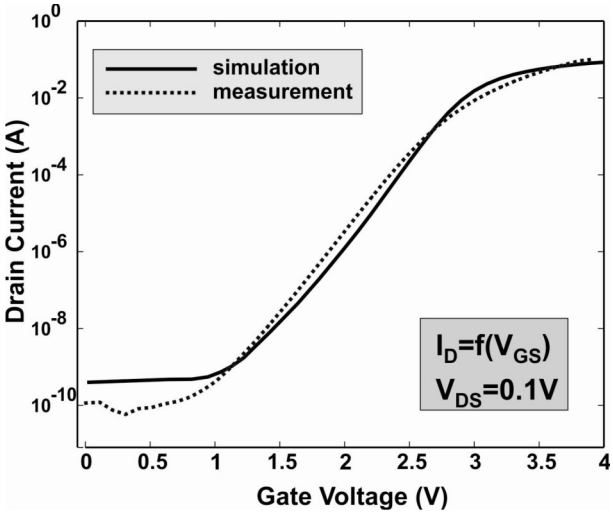

Figure 3: The measured and simulated transfer characteristics of power VDMOS transistor IRF510.

The major problem in the described procedure is to fit the gate oxide thickness, channel length and lateral channel doping profile, since they significantly influence on the device electrical characteristics. In addition, because the channel current flows vertically through the n-epitaxial layer and n^+ substrate to the drain contact (Fig. 2), considerable attention must be given to adjusting the vertical doping profile. Considering all of above data and facts the complete process flow is reconstructed and simulated by using the process simulator ATHENA. The obtained net doping

profile in two-dimensional (2D) simulation domain of power VDMOS transistor is also shown in Fig. 2.

The net doping profile is then used as input parameter for simulation of VDMOS electrical characteristics by using the device simulator ATLAS. Before the electrical simulation, it was necessary to calibrate the parameters of device simulators which largely depend on the specific technology characteristics, such as: fixed oxide charge density at the Si/SiO_2 interface, low-field electron and hole mobility, electron and hole velocity saturation, and electron and hole surface recombination velocities. Finally, a very good agreement of the measured transfer characteristics $I_D = f(V_{GS})$ for $V_{DS} = 0.1V$ and threshold voltage V_{TH} with simulation is obtained, as shown in Fig. 3.

3.2 The influence of semiconductor bulk traps on the electrical characteristics of power VDMOS transistor IRF510

As already mentioned, traps which are generated, for example, due to radiation or the application of high electric field on gate electrode of MOS transistor, can significantly affect on its electrical characteristics. As it is well known, in these cases the defects or traps are formed at the Si/SiO_2 interface, as well as in the oxide and semiconductor bulk.

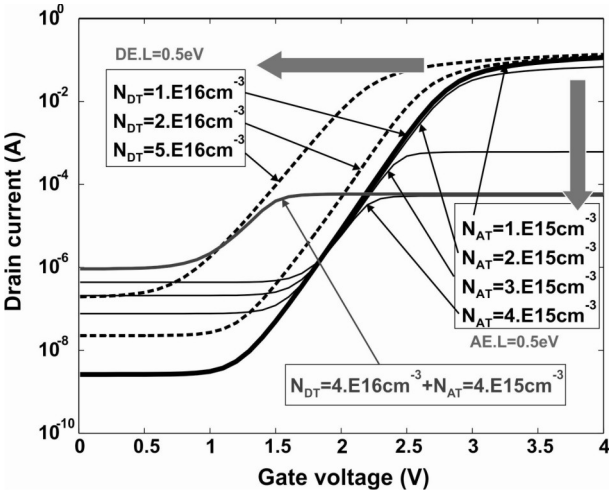

Figure 4: The influence of AT and DT density changes for fixed trap discrete energy levels (*DE.L*=0.5eV, *AE.L*=0.5eV) on power VDMOS IRF510 transfer characteristics.

The subjects of intensive research are the mechanisms of traps generation and the determination of their densities and charges (positive, negative or neutral) [8]. A particular problem is the separation of the effects of different types (DT or AT) and kinds (interface, oxide bulk or semiconductor bulk traps) of defects on the electrical characteristics, when a well-known experimental methods is used [9, 10]. This problem can be solved efficiently by using the existing TCAD software package tools, where it is possible to separate the influences of different types of defects on the device electrical characteristics. It is also possible to analyze the influence of generated defects on the potential, current density, recombination rate and carriers mobility distribution in the simulation domain.

At the beginning of TCAD analysis of semiconductor bulk traps influence on the electrical characteristics of power VDMOS transistor, it is important to recognize the role of DT and AT on threshold voltage, transconductance, leakage current, transfer and output *I/V* characteristics. In common MOS transistor, drain current flows only through the channel region and therefore only DT or AT influence on the electrical characteristics, depending on whether it is the n-channel or p-channel MOS transistor. In n-channel VDMOS transistors, as is noted above, the drain current after the channel, flows vertically through the n-epitaxial layer and n^+ substrate. In this case, DT has the dominant influence on the electrical characteristics in channel region, while AT reduces drain current when it flows vertically through the n epitaxial layer. To verify this assumption, we simulated the electrical characteristics of VDMOS transistor, firstly with DT, for different values of its densities N_{DT}, than with AT, for different values of its densities N_{AT}, and finally when both trap types are presented in semiconductor bulk. The obtained simulation results for given values of N_{DT} and N_{AT}, for fixed energy trap level values *DE.L=0.5eV* and *AE.L=0.5eV* are shown in Fig. 4. Based on the obtained electrical characteristics, it is obvious that when N_{DT} increases, the threshold voltage of VDMOS transistor decreases, while increasing of N_{AT} dramatically reduces the drain current. The leakage current increases in both cases.

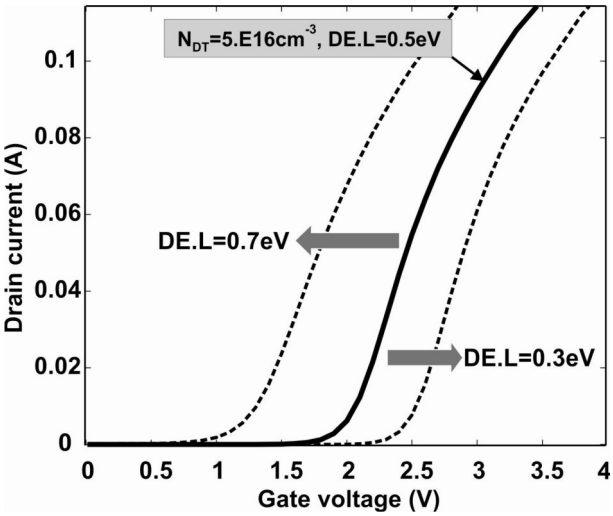

Figure 5: The influence of DT discrete energy level changes for $N_{DT} = 5.10^{16}$ cm^{-3} on power VDMOS transfer characteristics.

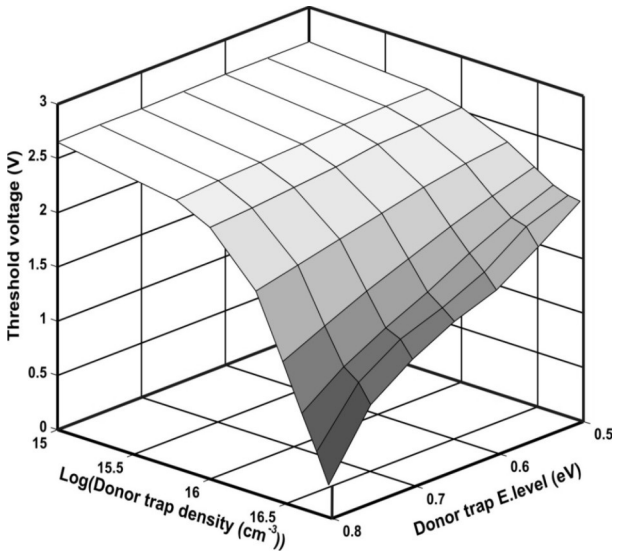

Figure 6: The changes of the threshold voltage of power VDMOS transistor.

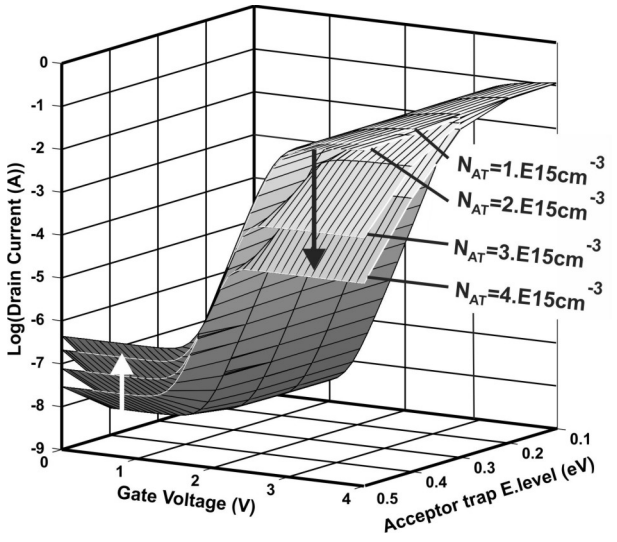

Figure 7: The influence of N_{AT} and *AE.L* on the drain current of power VDMOS transistor.

The influences of AT, when its densities N_{AT} change from 10^{15} to 4.10^{15} cm^{-3}, while the energy level position *AE.L* change from 0.1 to 0.5eV on the drain current are shown in Fig. 7. A dramatic decrease in the drain current with increasing density of AT is obvious. This is the effect of AT influence on the drain current in the n-epitaxial layer as it is discussed earlier. In Fig. 5 the influence of DT discrete energy level changes, for fixed trap densities 4. $N_{DT} = 5.10^{16}$ cm^{-3} is presented. It is obvious that when the value of parameter *DE.L* increases, which means that the donor-like trap energy level is closer to the bottom of the conduction band (Fig. 1.), threshold voltage decreases and at the same time the drain current increases. Vice versa, the threshold voltage increases, when the donor-like trap energy level is closer to the top of valence band. The changes of the threshold voltage, when the densities of N_{DT} are change in the range from 10^{15} to 10^{17} cm^{-3}, while the energy levels change from 0.5 to 0.8eV, are shown in Fig. 6.

4 Conclusion

In the design of integrated circuits, it is very important to know how the electrical characteristics of individual components are changed under the influences of various stresses. Defects which are generated at the Si/SiO_2 interface and in the semiconductor bulk and gate oxide have the dominant influence on the threshold voltage, drain current, transconductance and leakage current of MOS transistor. In this paper we simulate the impact of semiconductor bulk traps, which influences are commonly ignored in standard MOS structures, but in this case, due to the specific structure of the power n-channel VDMOS transistors, where the drain current flows vertically through n-epitaxial layer and substrate, it must be taken into account. Taking the advantage of TCAD software package, the impact of DT and AT influence on the electrical characteristics is simulated and analyzed separately, which is impossible to do with experimental results, where the influences of different mechanisms are mixed. Of course, a complete analysis of HEFS or radiation effect requires the simulation of the impact of the traps generated in gate oxide and at the Si/SiO_2 interface on the electrical characteristics of the power VDMOS transistor, which will be a matter of future work.

Acknowledgement

This work has been supported by the Ministry of Education and Science of the Republic of Serbia, under the project TR 33035.

References

1. Anghel C High Voltage Devices for Standard MOS Technologies – Characterisation and Modelling, Ph.D. Thesis No. 3116, Swiss Federal Institute of Technology, Lausanne (EPFL), Lausanne 2004.
2. Wang T, Chiang L, Zous N, Chang T, Huang C Characterization of Various Stress-Induced Oxide Traps in MOSFET's by Using a Subthreshold Transient Current Technique, IEEE Transaction on Electron Devices 1998; 45(8), 1791-1796.
3. Stojadinović N, Danković D, Manić I, Prijić A, Davidović V, Djorić-Veljković S, Golubović S, Prijić

Z Threshold voltage instabilities in p-channel power VDMOSFETs under pulsed NBT stress. Microelectron Reliab 2010; 50(9-11):1278-1282.
4. Alwan M, Beydoun B, Ketata K and Zoaeter M Bias temperature instability from gate charge characteristics investigations in n-channel power MOSFET, Microelectron. J 2007; 38, 727-734.
5. Karim N-M, Soin N, Banitorfian F, Manzoor S Analysis from the perspective of gate material under the effect of negative bias temperature instability, Informacije MIDEM 2012; 42(3): 176-184.
6. Benlatreche M.S, Rahmoune F, Toumiat O Experimental investigation of Si-SiO2 interface traps using equilibrium voltage step technique, Informacije MIDEM 2011; 41(3): 168-170.
7. Cijan G, Tuma T, Tomažič S, Birmen A Fast MOS transistor mismach optimization-a comparison between different approaches, Informacije MIDEM 2009; 39(1): 1-6.
8. Esseni D, Bude J-D, Selmi L On Interface and Oxide Degradation in VLSI MOSFETs—Part II: Fowler–Nordheim Stress Regime, IEEE Transaction on Electron Devices 2002; 49(2), 254-263.
9. Coelho A.V.P, Adam M.C, Boudinov H Distinguishing bulk traps and interface states in deep-level transient spectroscopy, Electroc. Solid State Lett. 2011; 14(9), 368-371.
10. Cartier E Characterization of the hot-electron-induced degradation in thin SiO_2 gate oxide, Microelectron. Reliab. 1997; 38(2), 201-211.
11. Xu H.P.E, Trescases O. P, Sun I.-S. M, Lee D, Ng W.T, Fukumoto K, Ishikawa A, Furukawa Y, Imai H, Naito T, Sato N, Tamura S, Takasuka K, Kohno T Design of a rugged 60 V VDMOS transistor, IET Circuits Devices Syst 2007; 1(5), 327–331.
12. Houssa M, Autran J L, Heyns M M and Stesmans A Model for defect generation at the (1 0 0) SiO2/Si interface during electron injection in MOS structures, Appl. Surf. Sci. 2003; 52, 212–213.
13. Zoaeter M, Beydoun B, Hajjar M, Debs M and Charles J-P Analysis and simulation of functional stress degradation on VDMOS power transistors, Act. Passive Electron Compon 2002; 25(3), 215-238.
14. Grasser T, Selberherr S Modeling of negative bias temperature instability, Invited paper, J. Telecom. and Inform. Technol 2007; 2, 92-102.
15. Aleksić S, Bjelopavlić D, Pantić D Simulation of bulk traps influences on the eleatrical characteristics of VDMOS transistors, In: Proc. TELSIKS 2011 Conf. 2011; 271-275.
16. *ATHENA User's Manual,* SILVACO, Inc., CA, USA, 2010.
17. *ATLAS User's Manual,* SILVACO, Inc., CA, USA, 2010.
18. Simmons J. G, Taylor G. W Nonequilibrium steady-state statistics and associated effects for insulators and semiconductors containing an arbitrary distribution of traps, Journal: Physical Review B 1971; 4(2), 502-511.
19. Law M, Solley E, Liang M, Burk D Self-consistent model of minority-carrier lifetime, diffusion length and mobility, IEEE Electron Device Letters 1991; 12(8), 401-403.
20. http://www.vishay.com/docs/91015/sihf510.pdf

Arrived: 09. 04. 2013
Accepted: 23. 05. 2013